DATASHEET

SMIC/CADENCE 90nm LOW-POWER DIGITAL REFERENCE FLOW FOR ENERGY-EFFICIENT SoC DESIGN

Based on Cadence® Encounter® technology, the SMIC/Cadence 90nm Low-Power Digital Reference Flow employs multiple supply voltages and advanced clock gating to facilitate the cost-effective design and manufacture of energy-efficient SoCs.

As the industry adopts process nodes at 90nm and below, three interdependent challenges have emerged: power consumption, manufacturability, and yield. Failed designs and production delays can cause millions of dollars in cost overruns, making the use of a complete, integrated, and reproducible RTL-to-GDSII flow essential. And to meet the growing demand for advanced handheld and portable devices that operate on sub-90nm process technologies, designers need a solution that supports low-power techniques to create high-performance and energy-efficient SoCs.

The SMIC/Cadence 90nm Low-Power Digital Reference Flow has been developed in response to these issues, delivering a high-yield, low-risk process that ensures the highest possible quality of silicon (QoS).

Validated in silicon, the SMIC/Cadence 90nm Low-Power Digital Reference Flow has been architected specifically to help you reduce power consumption. By using a sophisticated combination of advanced clock-gating techniques,support for multiple supply voltages within a single design, and the advanced low-leakage process developed by SMIC, you benefit from significant reductions in both dynamic and leakage power.

The SMIC/Cadence Reference Flow is based on an open-source processor that delivers a validated starting point for designers developing sub-90nm SoCs. Optimized for the SMIC 90nm Logic Low Leakage 1P9M process, the Reference Flow uses extensive IP developed by SMIC to deliver the highest QoS. The Reference Flow incorporates the following internally developed SMIC libraries:

- SMIC 90nm STD: SMIC DSD (scc09011_v12, scc090n11_v10)
- SMIC MEM: SMIC DSD (SPSRAM90n256x16, SPSRAM90n512x16)
- SMIC IO: SMIC DSD (SP90NLLD2_V0p1)
- SMIC 90nm Low-Power Kit: SMIC DSD (scc090n11_v12, scc090n11_v10_12)

The SMIC/Cadence Reference Flow also leverages the Cadence Encounter digital design platform, which boosts your productivity, helps you manage design complexity, and decreases your time to market. Three newly enhanced Cadence technologies, however, are central to the Reference Flow:

- Encounter Test: a three-product suite with optimal compression and physically aware diagnostics capabilities that delivers a faster, more cost-effective single-pass diagnostics flow and accelerates yield ramp
- NanoRoute® Ultra: a routing solution that allows you to employ concurrent multi-cut via insert and wire spreading, two sophisticated techniques for developing more reliable designs
- Encounter Timing System: a comprehensive signoff verification system that combines accurate delay calculation, effective current source modeling, and global timing debug

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BENEFITS

- Delivers a validated flow, fully compatible with the leading-edge SMIC 90nm Logic Low Leakage 1P9M 1.2/1.8/2.5V process
- Provides custom-architected, internally developed SMIC libraries and IP to streamline the SoC design process
- Uses Encounter Timing System to provide a full-chip, gate-level timing/signal integrity analysis and signoff verification that combines accurate delay calculation, advanced modeling, and global timing debug
- Leverages Encounter RTL Compiler to resolve timing, area usage, and power issues concurrently, providing higher QoS and more efficient power utilization
- Supports multiple supply voltages to reduce dynamic power by up to 30% (by reducing supply voltage from 1.2V to 1.0V within selected portions of the design)
- Uses NanoRoute Ultra to enable concurrent multi-cut via swap and wire spreading to increase manufacturability, reliability, and yield
- Employs VoltageStorm® technology to perform flat and hierarchical power-grid analysis and signoff of cell-based designs, such as custom ICs, ASICs, and SoCs

FEATURES

The SMIC/Cadence 90nm Low-Power Digital Reference Flow provides SoC developers with a validated and predictable RTL-to-GDSII development path based on comprehensive, integrated Cadence Encounter technologies. All key processes in the flow are optimized, including power utilization, timing closure, signal integrity analysis, and area reduction. A wide range of Cadence digital design and verification technologies implement the flow and support the creation of successful SoCs at each stage of the design cycle, enhancing manufacturability and yield.

LOGIC SYNTHESIS

Encounter RTL Compiler logic synthesis delivers higher-quality netlists in less time with less effort. This advanced synthesis solution provides several key benefits, starting with improved quality of silicon in terms of power optimization, timing closure, and enhanced area utilization. Dramatically faster runtimes and higher overall capacity help you work more effectively. With new global optimization algorithms, Encounter RTL Compiler performs single-pass concurrent synthesis for meeting timing, area, and power targets to create low-power, multi-million gate designs. Coupled with Encounter Test's clock gating and power optimization techniques, Encounter logic synthesis streamlines the front-end design process.

SILICON VIRTUAL PROTOTYPING

Based on the SoC Encounter implementation system, silicon virtual prototyping is the cornerstone of the SMIC/Cadence Reference Flow, providing you with a more efficient method of validating your design assumptions and constraints. Because silicon virtual prototyping delivers immediate feedback on the SoC's timing, congestion, and power consumption, design time is significantly shorter than when performing a complete place-and-route iteration.

HIERARCHICAL FLOORPLAN GENERATION

SoC Encounter™ technology uses a hierarchical methodology to facilitate chip implementation. Hierarchical floorplanning decisions can be finalized after the silicon virtual prototyping phase is completed. Hierarchical floorplan generation defines the top-level floorplan and blocks within that floorplan that can be implemented separately for increased design control.

EQUIVALENCE CHECKING

Conformal® Equivalence Checker is used throughout the flow to check functional equivalence of two versions of a design, helping you identify and correct errors quickly.

IMPLEMENTATION

Top-level implementation involves placement, in-place optimization, clock-tree synthesis, and routing. It follows after all blocks are implemented and where standard block models are generated. Physical synthesis can be launched for timing closure on the most difficult blocks.

Global Physical Synthesis

SoC Encounter technology combines silicon virtual prototyping with high-performance physical synthesis capabilities that leverage Encounter RTL Compiler's patented global physical synthesis (GPS). Unlike traditional approaches that optimize a single logic path at a time, GPS optimizes the timing of multiple paths concurrently. This approach reduces the amount of time and effort required to reach design convergence. GPS also optimizes both RTL-to-placement and netlist-to-placement flows.

Low-Power Optimization

Scalable multi-Vdd (MSV) infrastructure is an advanced low-power technique that reduces power usage dynamically by supplying different power voltages to different parts of the design. With its advanced, single-pass, domain-aware synthesis capabilities, Encounter RTL Compiler can achieve optimal results for all power domains simultaneously. The SoC Encounter system then enables flat and hierarchical MSV implementations of the design, with power-aware timing and signal integrity optimization.

Signal Integrity (SI) Closure

NanoRoute Ultra provides an SI–aware routing solution with built-in design-for-manufacturability capabilities to achieve rapid SI closure. It takes advantage of scripts incorporated into the SMIC/Cadence 90nm Low-Power Digital Reference Flow, allowing you to use advanced techniques such as multi-cut via swap and wire spreading to increase reliability and manufacturability. Multi-cut via swap adds redundancy by increasing the number of interconnect cuts for vias at key points in the design, and wire spreading separates key pathways to prevent crosstalk or bridging from occurring.

CHIP ASSEMBLY AND SIGNOFF

The SMIC/Cadence 90nm Low-Power Digital Reference Flow uses Fire & Ice® QXC signoff extractor to validate the timing of nanometer designs while enabling detailed signal integrity verification. The flow also emlpoys VoltageStorm power-grid verification to ensure you meet your power requirements. Encounter Timing System provides a comprehensive signoff solution including signal integrity analysis, IR-drop–aware and accurate delay calculation, advanced modeling, and global timing debug. Conformal Equivalence Checker then completes the SoC assembly and signoff process.

CHIP FINISHING

Fully interoperable with the Encounter digital design platform, Virtuoso® Chip Editor provides high-performance editing for full-chip finishing tasks on even the largest designs, dramatically reducing the time to reach tapeout. Assura® DRC/LVS then performs physical verification to identify design rule errors prior to manufacturing tapeout.

FOR MORE INFORMATION

To learn more about how Cadence and SMIC are collaborating to facilitate your success, visit www.cadence.com/partners/foundry_program/smic.aspx or email us at foundry_support@cadence.com.

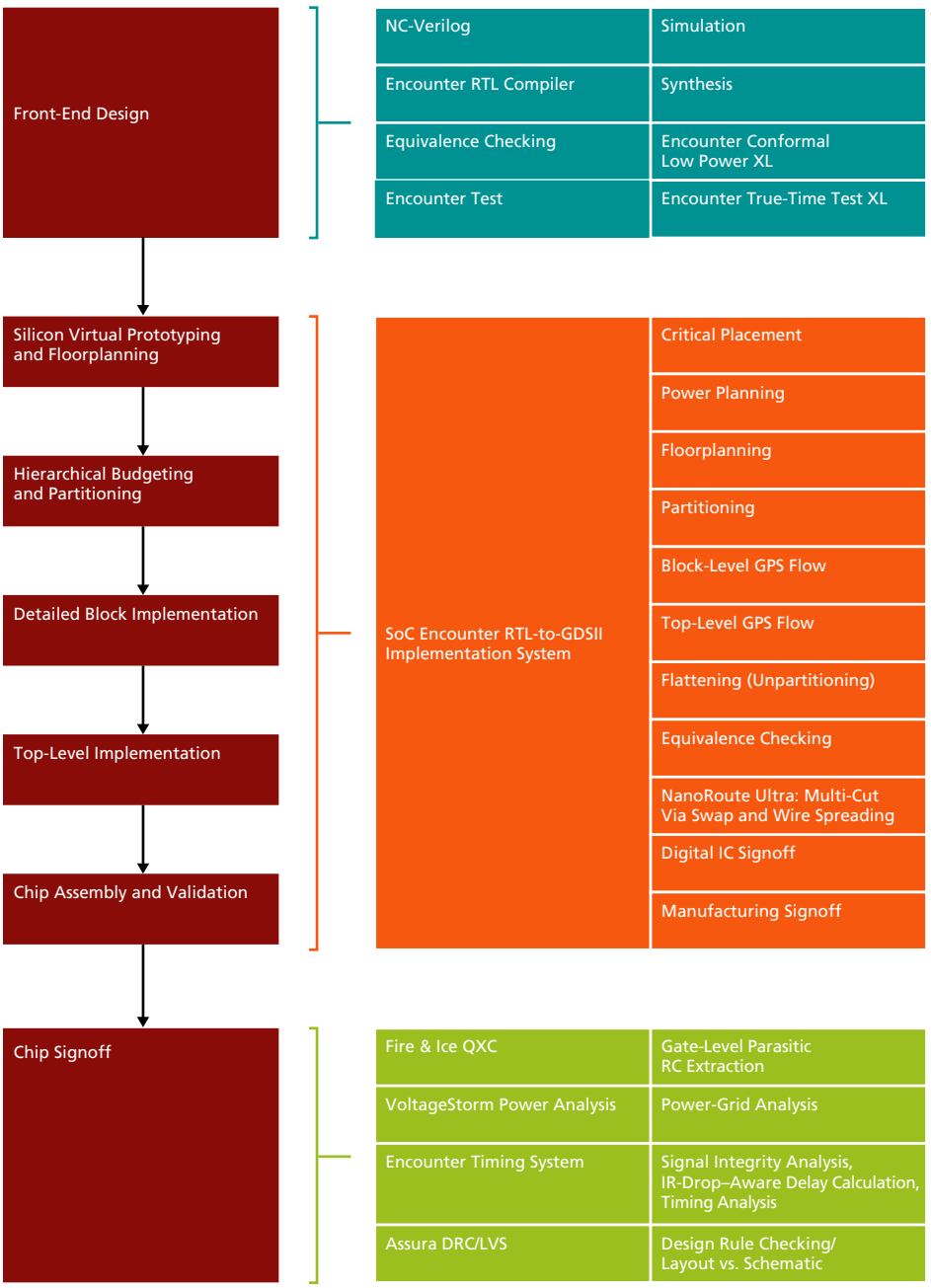

Figure 1 : The SMIC/Cadence 90nm Low-Power Digital Reference Flow

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