Cadence Reference Flow for the IBM-Chartered 90 nm CMOS process streamlines design of SoCs.

Today's ever-increasing silicon integration means more is riding on each design – often including make-or-break business issues for your company. In a world where failure is not an option, 90 nm SoC design teams require methodologies and tools capable of handling the enormous capacity requirements, low power optimization, nanometer test challenges, and signal integrity issues intrinsic to these projects.

The Cadence Reference Flow for the IBM-Chartered 90 nm CMOS process streamlines the design of system-on-chip (SoC) devices with exceptional Quality of Silicon (QoS). By shortening the path from RTL to GDSII, this innovative, pre-tested approach, based on the Cadence Encounter digital IC design platform, is designed to enhance design team productivity and silicon reliability, and to accelerate time-to-volume.

Reference Flow overview

The Cadence Reference Flow for the IBM-Chartered 90 nm CMOS process provides SoC developers with an optimized RTL-to-GDSII flow.

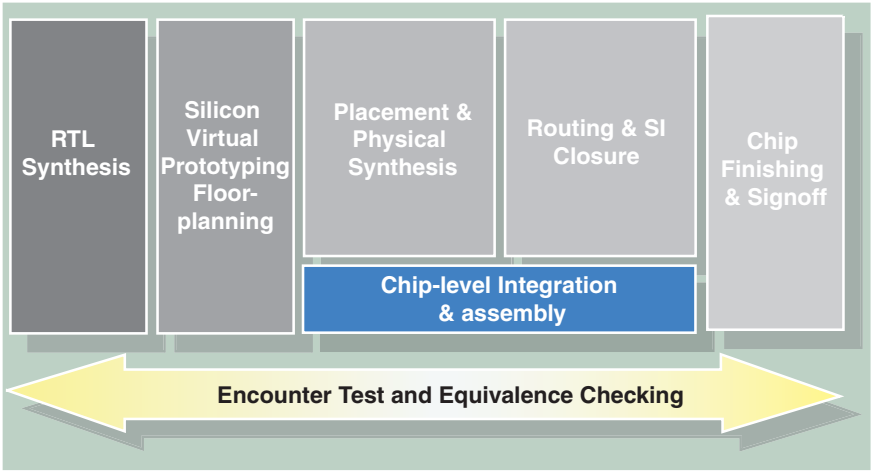
Based on the Cadence Encounter Platform, this advanced flow replaces traditional linear design flows with a completely new design strategy that can minimize time to wires and full chip iteration time to ensure the highest QoS. A nanometer router optimizes wire creation for performance and manufacturability, and a unified database has the capacity needed to support designs up to 50 million gates.

SoCs can be developed from floorplan through to silicon by the design team and/or by incorporating third-party IP validated with the flow.

The Quality-of-Silicon (QoS) metric

As SoC designs move towards 90 nm, new metrics for speed, area, power, and test are needed. QoS has emerged as the metric that exclusively handles measurements after wires. This new metric provides a mechanism for accurately measuring speed, area, and power offered by a netlist, and adds value at all stages of the design flow.

The capability to seamlessly integrate IP from multiple sources can lead to increased design efficiency and quicker time-to-silicon.



Reference Flow overview

Highlights

- ***Replaces traditional linear design flows with a completely new design strategy that minimizes time to wires and full chip iteration time to deliver high QoS***
- ***"Wires-first" technology designed to optimize area utilization, power consumption, timing and test coverage***
- ***New-generation global synthesis technology supports high capacity and run-time requirements of nanometer designs using over 50 million gates***
- ***Incorporates an at-speed structural nanometer test solution to improve QoS and yields***
- ***Validated as compatible with the IBM-Chartered 90 nm CMOS process platform***

Encounter Digital IC Design Platform	
Tool	**Purpose**
Encounter™ RTL Compiler	RTL synthesis
Encounter Test	DFT test generation, diagnostics
First Encounter® Ultra	Silicon virtual prototyping & physical synthesis
Incisive™ Conformal	Equivalence checking
NanoRoute™ Ultra	Routing
CeltIC™	SI closure
VoltageStorm®	Power analysis
Fire & Ice® QXC	Interconnect extraction
Assura™ DRC/LVS	Physical verification

Encounter RTL Compiler

A key component of the Encounter platform, Encounter RTL Compiler, uses a unique, patented set of global optimization algorithms to maximize QoS for high-speed nanometer designs. Encounter RTL Compiler achieves timing closure by identifying key leverage regions in the design and working on multiple paths simultaneously, and by effectively leveraging the target process library. This global synthesis technology provides a better netlist for the back-end in less time than legacy tools, generating outstanding results at each stage of the implementation – including a better starting point for routing complex, wire-centric designs.

The Encounter RTL Compiler global optimization algorithms offer a new approach for creating low-power designs by enabling single-pass power and timing optimization. In addition, enhanced area utilization reduces die size, offering design teams a more predictable and cost-effective path to silicon.

As a new generation of multi-million gate 90 nm SoCs pushes the timing and power limits of the 90 nm process node. Designers need front-end tools that are both innately faster and capable of creating netlists that ease back-end implementation. Encounter RTL Compiler excels in both areas, delivering dramatically faster run times than traditional synthesis tools, and a netlist that is optimized for placement and routing. Full backward-compatibility enables designers to quickly upgrade from older synthesis tools based on quality of results (QoR) measurements. The net result is that Encounter RTL Compiler can help designers achieve high QoS levels in less time and with less effort.

Comprehensive power solution

The IBM-Cadence 90 nm Reference flow provides designers with a comprehensive approach to power management, a critical concern in 90 nm technology. By offering insight into power management at every stage of the reference flow, design teams are able to more fully address the issues surrounding power reduction and optimization.

The Encounter platform provides a robust power planning environment to drive implementation:

- Gate-level switching optimization reduces dynamic power consumption during place and route.
- Built-in features are designed to reduce power and to balance skew during clock tree synthesis.
- Leakage power is reduced throughout the flow through full support of multi-voltage threshold libraries.
- VoltageStorm analyzes the integrity of the power grid.

Encounter Test Solutions

In environments where production delays can cost millions of dollars, quick and accurate testing in both design and manufacturing are absolutely essential. Cost-of-test can make the difference in a design reaching profitability, making efficient testing throughout the design and manufacturing process a critical component of success. Based on Cadence's deterministic transition fault methodology, Encounter Test is designed to deliver high QoS levels, solid designs, and high yields in the manufacturing process.

By maximizing stuck-at and transition fault coverage and minimizing test vectors, Encounter Test solutions deliver superior Quality of Silicon while continuing to contain costs. Available in separate versions for design and manufacturing environments, this applications address the entire testing process from insertion and analysis through test generation to physical failure analysis. The comprehensive tools suite delivers a wide range of fault-modeling capabilities that provides testing and diagnosis of timing faults, bridges, and an extensible model for attacking other failure mechanisms prevalent in nanometer designs.

Encounter Test Design Edition

Created for the pre-GDSII design environment, Encounter Test Design Edition features an intuitive graphical user interface that guides designers through the test insertion, testability analysis, and test generation processes. The software includes support for managing the complexities of modern SoC designs, including core-based hierarchical testing, Memory BIST, and I/O testing. The application suite can help design teams achieve faster time-to-market, better test coverage with advanced ATPG algorithms, and an overall reduction in cost-of-test.

Silicon Virtual Prototyping

First Encounter-based Silicon Virtual Prototyping (SVP) is the cornerstone of the IBM-Cadence flow, enabling designers to rapidly go through the implementation steps necessary to validate their assumptions and constraints in designs as large as 50 million gates. Because the SVP process delivers immediate feedback on the timing, congestion, and power consumption of the design, design time can be reduced by an order of magnitude from that of performing a complete place-and-route iteration.

A predictable path to silicon

In an environment where delays in design, testing, or manufacturing can easily make the difference between profitability and costly re-spins, it is essential to eliminate as many variables as possible. The Cadence Reference Flow uses the synergy between advanced 90 nm IBM-Chartered process technology and the Cadence Encounter platform to deliver a validated flow that can be closely monitored and assessed during the design process. This predictable path to silicon is designed to shorten design cycles, provide higher levels of QoS, and ensure that projects stay on track and on budget.

Placement and physical synthesis

Physical synthesis enables timing closure of even the most difficult blocks, including clock tree synthesis that generates the clock network in terms of both clock skew and insertion delay.

Routing and SI closure

The SI-aware NanoRoute application uses built-in design for manufacturability (DFM) capabilities to perform routing and signal integrity closure. The routing resulting from NanoRoute has minimal signal integrity violations and has been demonstrated to meet timing and manufacturability constraints in hundreds of tapeouts. The SI closure loop, which is performed using the CeltIC signal integrity analyzer, eliminates any remaining SI violations from the design.

Chip-level Integration and assembly

The Cadence Reference Flow for the IBM-Chartered 90 nm CMOS process facilitates implementation of the chip using a hierarchical methodology. Chip-level integration and assembly are supported in the same environment using standard block models for top-level integration. Functions include top-level zero-skew clock tree synthesis and top-level timing optimization.

Chip-level analysis and sign-off

The Cadence Reference Flow for the IBM-Chartered 90 nm CMOS process uses the Fire & Ice QXC sign-off extractor to validate the timing of designs while enabling detailed signal integrity verification. The flow also uses the industry-standard power grid verification tool – VoltageStorm – to ensure that power requirements are met. Physical verification is performed by Assura to identify design rule errors prior to taping-out to manufacturing.

Equivalence checking

The Cadence Incisive Conformal logic equivalence checker is used throughout the flow to check functional equivalence of two versions of a design, enabling errors to be quickly identified and corrected.

Cadence Engineering Services

Because even the largest and most competent design organizations sometimes require help, Cadence Engineering Services is poised to assist you in implementing part or all of this reference methodology into your team's design environment. More information about Cadence Engineering Services is available at: http://www.cadence.com/engr_services.

To learn more

Find out more about how Cadence, IBM and Chartered are partnering to enable your success by visiting: *http://www.cadence.com/partners/foundry_program/ibm.aspx*
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