DATASHEET

UMC-CADENCE DIGITAL REFERENCE FLOW

Executive Summary

The UMC-Cadence Digital Reference Flow is an Encounter-based solution that provides SoC developers designing at 130nm and below with a pre-qualified, predictable path to silicon. This flow is based on an open-source processor that delivers a validated starting point for creating SoCs. Optimized for UMC's leading-edge 0.13um Logic HS/FSG process, the flow uses Faraday's libraries, memory blocks, and other intellectual properties (IP) to provide high Quality of Silicon (QoS) levels in terms of power, timing closure, signal integrity, and reduced area usage.

By providing a totally integrated solution capable of supporting large, hierarchical or flat designs, the flow improves design team productivity and offers a faster, reduced-risk path to silicon. Key Cadence technologies utilized in implementing the flow include Encounter™ RTL Compiler, First Encounter, Global Physical Synthesis (GPS), NanoRoute™, Incisive Conformal®, VoltageStorm™, Fire & Ice QX, Virtuoso™ Chip Editor, and Assura.

- Validated as fully compatible with UMC's leading-edge 130nm Logic HS/FSG process
- Enhanced QoS provides designs with better timing, reduced area usage and lower power consumption
- RTL Compiler provides new generation logic synthesis technology that delivers high QoS, enhanced capacity, and faster runtimes
- Offers comprehensive power optimization and analysis capabilities that are critical for meeting demands of designs at 130nm and below
- Supports runtime and capacity demands of designs at 130nm and below using over 50 million gates

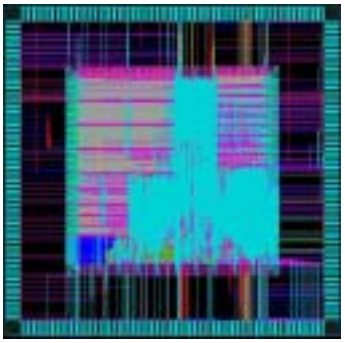

Figure 1: The UMC-Cadence Digital Reference flow based on open-source processor offers a validated starting point for the creation of highly-customized, sub-130 nanometer SoCs.

The need for SoC design acceleration techniques capable of meeting the pressures caused by tightening time-to-market cycles is of critical importance. Increased time pressure and the threat of cost overruns in both design and manufacturing has heightened the urgency for uncovering and correcting potential problems early in the physical design cycle. Failed designs and production delays have the potential of causing cost overruns that can run into millions of dollars, making the use of a complete, integrated, and reproducible RTL-to-GDSII flow essential.

The Encounter-based UMC-Cadence Digital Reference Flow is capable of supporting large, hierarchical or flat SoC designs, and delivers high QoS levels in terms of low power, timing improvement, and enhanced area utilization. In addition, the flow speeds development by reducing the number of cycles needed to reach design closure, solving signal integrity, timing closure and IR drop problems early in the design process. This streamlined path to silicon enables developers to create large SoC designs in a timely and cost-effective manner, and avoid the risks associated with a potential design failure.

To facilitate the cost-effective development of highly-customized SoCs, Cadence and UMC have developed and verified an open-source, sub-130nm test design. This test design was taped out to be proven in silicon, and serves as a verified base for customers to develop their own SOC designs. The test chip follows the reference flow that incorporates UMC's 0.13um Logic HS/FSG process and Faraday's libraries, memory blocks, and IP.

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The UMC-Cadence Digital Reference Flow provides SoC developers with a predictable and validated RTL-to-GDSII development path. Based on the Cadence Encounter Platform, a complete and tightly integrated design and verification platform, the flow delivers an effective hierarchical RTL-to-GDSII IC solution for nanometer design processes at 130nm and below.

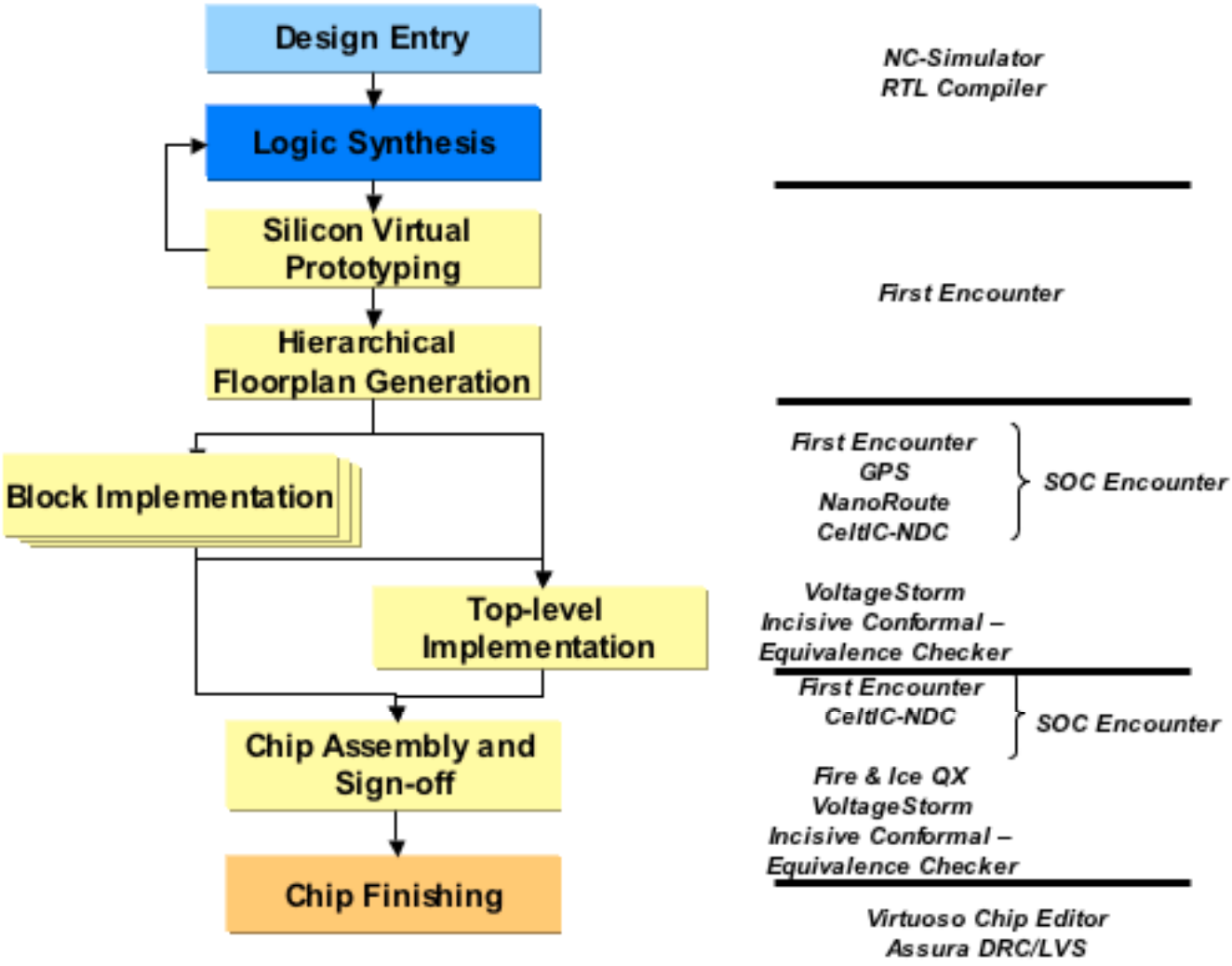

Figure 2: UMC-Cadence Digital Reference Flow.

The UMC-Cadence Digital Reference Flow includes the following key development and verification technologies:

Logic Synthesis

Encounter™ RTL Compiler Synthesis delivers higher-quality netlists in less time with less effort. This advanced synthesis solution provides several key benefits, starting with improved QoS in terms of power optimization, timing closure and enhanced area utilization. Dramatically faster runtimes and higher overall capacity enables design teams to work more effectively. And with new global optimization algorithms, Encounter RTL Compiler offers an enhanced approach for creating low-power, multi-million gate designs.

Silicon Virtual Prototyping

First Encounter-based Silicon Virtual Prototyping (SVP) is the cornerstone of the UMC-Cadence flow, providing designers with a streamlined method of validating their design assumptions and constraints. Because the SVP process delivers immediate feedback on the timing, congestion, and power consumption of the SoC, design time can be reduced by an order of magnitude from that of performing a complete place-and-route iteration.

Hierarchical Floorplan Generation

First Encounter uses a hierarchical methodology to facilitate chip implementation. Hierarchical floorplanning decisions can be finalized after the Silicon Virtual Prototyping phase is completed. Hierarchical Floorplan Generation defines the top-level floorplan, and blocks within that floorplan that can be implemented separately for increased design control.

Equivalence Checking

The Cadence Incisive Conformal® logic equivalence checker is used throughout the flow to check functional equivalence of two versions of a design, enabling errors to be quickly identified and corrected.

Blocks and Top-level Implementation

Top-level implementation involves placement, in-place optimization, clock-tree synthesis, and routing. It follows after all blocks are implemented, and where standard block models are generated. Physical synthesis can be launched for timing closure of the most difficult blocks.

- First Encounter Global Physical Synthesis combines silicon virtual prototyping with high-performance physical synthesis capabilities that leverage Cadence RTL Compiler's patented global-focused synthesis technology. Unlike traditional physical synthesis approaches that optimize a single logic path at a time, GPS is capable of optimizing the timing of multiple paths simultaneously. This approach reduces the amount of time and effort required to reach design convergence. GPS is capable of optimizing both RTL-to-placement and netlist-to-placement.

- Signal Integrity (SI) Closure is achieved by the SI-aware NanoRoute™ routing solution, which features built-in "design for manufacturability" (DFM) capability. Routing resulting from NanoRoute has minimal signal integrity violations and has been demonstrated to meet timing and manufacturability constraints in many tapeouts. The SI closure loop, which is performed using CeltIC™-NDC, eliminates any remaining SI violations from the design.

Chip Assembly and Sign-off

The UMC-Cadence Reference Flow uses the industry's most accurate sign-off extractor—Fire & Ice QX. This provides a well-proven solution for accurately validating the timing of nanometer designs while enabling detailed Signal Integrity verification. The flow also uses the industry standard power grid verification tool—VoltageStorm™—to ensure that power requirements are met.

Chip Finishing

Fully interoperable with the Cadence Encounter™ digital IC design platform®, Virtuoso® Chip Editor Physical provides high-performance editing for full-chip finishing tasks on even the largest designs, dramatically reducing the time required for tapeout tasks. Physical verification is performed by Assura to identify design rule errors prior to taping-out to manufacturing.

To learn more Find out more about how Cadence and UMC are partnering to enable your success by visiting: http://www.cadence.com/partners/foundry_program/umc.aspx or by contacting us at: Mailto:foundry_support@cadence.com.

To gain access to the detailed flow, log on to my.umc.com, or contact us at digital_flow_support@umc.com